PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Noriaki ODA

Appln. No. 09/739,620 Group Art Unit: 2812

Confirmation No.: 4739 Examiner: Ha Nguyen

Filed: December 20, 2000

For: SEMICONDUCTOR DEVICE WITH COPPER-BASED WIRING LINES AND METHOD OF FABRICATING THE SAME

EXCESS CLAIM FEE PAYMENT LETTER

Commissioner for Patents
Washington, D.C. 20231

Sir:

An Amendment Under 37 C.F.R. § 1.111 is attached hereto for concurrent filing in the above-identified application. The resulting excess claim fee has been calculated as shown below:

	After Amendment		Highest No. Previously Paid For						
All Claims	25	-	24	=	1	X	$18.00	=	$18.00
Independent	3	-	3	=		X	$84.00	=	$.00
					TOTAL			=	**$18.00**

A check for the statutory fee of $18.00 is attached. Please charge any additional fee or credit any overpayment to our Deposit Account No. 19-4880. A duplicate copy of this letter is enclosed.

Respectfully submitted,

David A. Klein

David A. Klein
Registration No. 46,835

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Date: **December 26, 2001**

#8/Amdt A
Q. Toal
1/4/01

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Noriaki ODA

Appln. No.: 09/739,620

Confirmation No.: 4739

Group Art Unit: 2812

Filed: December 20, 2000

Examiner: Ha Nguyen

For: SEMICONDUCTOR DEVICE WITH COPPER-BASED WIRING LINES AND METHOD OF FABRICATING THE SAME

AMENDMENT UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated September 26, 2001 please amend the above-identified application as follows:

IN THE CLAIMS:

Please enter the following amended claims:

1. (Amended) A semiconductor device comprising:

(a) a substrate having a surface;

(b) a dielectric formed over the surface of the substrate; and

(c) a wiring line buried in the dielectric;

the wiring line including a Cu-based conductor and a first cover layer covering an outer surface of the conductor;